Open Graphics Project

Product Specification

This document describes a preliminary feature set for the Tech Source Open Graphics card. It is being published as a status update and as a call for more feedback from the community so that we can identify any important features which may be missing. It is important to note that this is a proposed, *unapproved* specification, meaning that it hasn't been evaulated by management, and there are no guarantees that any listed features will appear in the final product.

Physical component break-down

PCB	• half-height/half-length PCI version • half-height/half-length AGP version (probably)
GPU	Xilinx Spartan III 1500 FPGA
ROMs	• BIOS/firmware • Serial prom for FPGA
RAM	128 Megabytes (four 256 megabit chips)
Video	DVI-I providing both digital and analog
Host interface	PCI and AGP
Misc.	DVI-I connector, face plate, power supply, general (user) I/O pads

GPU component break-down

Host interface	• PCI and (probably) AGP 4x versions • DMA for rendering commands • YUV<->RGB conversion • Emulation of 8-bit and 16-bit framebuffer pixel sizes • Bit swapping for big-endian/little-endian conversion • Some MesaGL security features (possible feature) • Interrupts for rendering and DMA state changes
Video	• Single channel (multi-channel in future) • Fully programmable, supporting VESA, DVI reduced-blanking, progressive scan, interlaced, etc. • Up to 250Mhz (165Mhz for DVI) pixel clock • Single 64x64 full-color alpha-blended hardware cursor • Integer scaling (possible feature) • Window-ID, 8-bit overlay, dual-LUT • Vertical interrupts

Memory	• Quad-channel 400Mhz DDR • Maximum total bandwidth: 1.6 billion pixels/second • Linear and tiled addressing • DMA bypass for accessing host images
VGA	• 80x25 text, 640x480x16, etc. • Can be disabled for secondary cards
3D renderer	Support for basic 3D rendering plus extensions for 2D (see below)
Misc.	PROM reading/writing interface, peripheral bus, user-programmable I/O

Rendering engine features

Data format	• All rendering coordinates are in 16.16 fixed point. • All colors are in 8.8 fixed point. • Framebuffer pixels are always 32-bit ARGB
Performance	• Dual-pixel pipeline at 200 Mhz • 400 million pixels/second [*] • Triangle rate limited by host interface speed
Gouraud shading	• Simple linear interpolation • Second-order differential for approximation of Phong shading (possible feature)
Texture mapping	• Simple linear interpolation • Second-order differential for approximation of perspective correction (possible feature) • Bilinear interpolation
Antialiasing	Power-of-two super-sampling
Other 3D features	• Z-buffering (32-bit) • Fog • Alpha test • Alpha blend • Arithmetic raster-op • Stencil/Mask/Color key
2D features	• Polylines (solid and patterned) [**] • Plane mask • Logical raster-op (GDI ROP4) • Patterns (8x8 color, 32x32 mono) • Rectangular clipping

Open Source software

- Linux drivers (DRI, X.org, MesaGL) under BSD+MIT+GPL licenses
- Windows drivers (if possible, considering IP constraints)
- x86 PC BIOS
- Sun OpenBoot

NOTES

[*] Different parts of the pipeline attempt to access memory simultaneously. There is a total bandwidth limit of 1.6 billion pixels/second. This means that although a bitblt/texture operation doubles the memory bandwidth requirement as compared to as solid fill (read 400MP/s and write 400MP/s, for a total of 800MP/s), the pipeline will still operate at full speed because the limit of 1600MP/sec hasn't been reached.

[**] Having a unified pipeline, most 2D rendering primitives are drawn as special cases of 3D primitives.